## REMARKS

Claims 1-9 are all the claims originally pending in the application. Claims 1-5 have been rejected. Claims 6-9, which were withdrawn from consideration on the basis of a restriction requirement, have been cancelled without prejudice or disclaimer. New claim 10 has been added. Claims 1-4 have been amended.

### *Election/Restriction*

In response to the Examiner's requirement for restriction under 35 U.S.C. § 121, Applicant elected claims 1-5 for examination. Claims 6-9 have been withdrawn from consideration by the Examiner. Applicant has canceled claims 6-9 without prejudice or disclaimer, particularly with respect to the filing of one or more divisional applications on the non-elected inventions.

### *Claim Objections*

Claim 1 is objected to because certain phrases at lines 5-6 do not have a stated antecedent basis. The claim has been amended to overcome this objection.

### *Claim Rejections - 35 U.S.C. § 103*

**Claims 1 and 3-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kito et al (6,110,279) in view of Cook et al (6,352,594).** This rejection is traversed for at least the following reasons.

**The Invention**

As a preliminary matter, Applicant notes that an object of the present invention is to produce a thick SiC single crystal that is low in planar defect density and impurity concentration, and thus, desirable for use in semiconductor devices. In achieving that object, the invention involves depositing a high-quality SiC layer on a substrate surface, while avoiding undesirable etching of the substrate surface by an impurity gas during an early stage of growth of the SiC layer.

To this end, prior to deposition of the SiC layer, the substrate surface is carbonized or silicified so that the substrate surface has formed thereon an initial thin single crystal SiC layer or film, which acts to prevent the substrate surface from being etched by the impurity gas during the subsequent deposition of the thick SiC layer. In an exemplary embodiment, the thin single crystal SiC layer or film is formed by substrate surface reaction, where the substrate has at least

one of Si or C. A schematic illustration of the process is presented in the sequence of Figs. 1A-1C, and the description thereof beginning at page 8 of the present application.

The inventive method is recited in claim 1, as amended herein for clarity, which sets forth two steps in the process:

> The first step involves coating a substrate having at least one of Si or C with a single crystal layer or film of SiC by inducing a surface chemical reaction between the raw material and Si or C contained in the substrate. The terms thin layer or "film" is used to distinguish the thin single crystal SiC layer (for example, layer 101a in Fig. 1C) from the deposited thicker SiC layer (for example, layer 101b in Fig. 1C). The term "surface chemical reaction" is supported by the description in the specification at page 11, lines 1-17, which describes the formation of the SiC layer using Si as the substrate and $C_2H_2$ as the material gas, in conjunction with Figs. 3 and 4. In this case, a silicon source is not contained in the material gas. From this teaching, one of ordinary skill would directly and unambiguously understand that the SiC layer is produced by the reaction which takes place above the substrate surface between Si in the substrate surface and $C_2H_2$ as the material gas. All of the embodiments described in the present specification are related to the formation of a SiC film by such surface chemical reaction. Also, in this step, the partial pressure of the raw material gas is higher by a predetermined rate than that of an impurity, which further prevents the etching of the substrate surface by the impurity gas.
>
> Thereafter, in a second step, SiC is deposited in a thick layer by vapor phase growth or liquid phase growth on the thin single crystal SiC layer or film, formed in the first step.

This process clearly differs from the prior art cited by the Examiner, as subsequently detailed. Moreover, the difference is further amplified by the recitation in dependent claim 2 that the first step involves a particular temperature elevating protocol where the predetermined partial pressure is not lower than a 100 times that of the impurity gas. The remaining dependent claims 3-5 and 10 specify further details of the method.

**Kito et al**

Kito et al concerns a method of producing a (0001) α-type SiC single crystal ingot 19 on a (111) cubic single-crystal silicon carbide layer 15 at high temperatures, well above the melting point of silicon substrates.

Specifically, in the third embodiment referenced by the Examiner (Figs. 13-19) to support his rejection, Kito et al discloses growing a (111) cubic silicon carbide crystal layer 15 on a silicon wafer 14 and growing (0001) α-type SiC single crystal layer 19a on the (111) cubic silicon carbide single-crystal layer 15 by a CVD method (col. 12, line 64-col. 13, line 11). Then, a (0001) α-type SiC single crystal ingot 19 is formed on layer 19a by a sublimation-recrystallization method (col. 13, lines 16-21). In this process, use is made of a base layer having a double-layer structure including (0001) α-type SiC single crystal and (111) cubic SiC single crystal. Notably, the double-layer base layer is deposited by CVD using $SiH_4$ and $C_3H_8$ as raw material gases. Other techniques also can be used for depositing such layer, as disclosed at col. 14, lines 37-46, but none involve surface chemical reaction of the substrate.

In the preferred method of the third embodiment, in the process of depositing the (111) cubic SiC single crystal 15 onto the silicon substrate 14 by CVD, the silicon substrate 14 temperature during deposition is 1300°C. The silicon substrate temperature can be adjusted within a range not higher than 1400°C, which is the melting point of Si (col. 12, lines 30-46). When depositing the (0001) α-type SiC single crystal 19a by CVD, the (111) Si single crystal substrate 15 temperature is adjusted to 1500°C, which is above the melting point of silicon. Finally, the silicon substrate 14 is removed after mounting the combined layers 14 and 15 onto a support plate 30, and the deposition of the ingot 19 onto the layer 19a is accomplished at temperatures of at least 1500°C and up to 2000°C (col. 12, line 64-col. 13, line 4). This process permits optimum formation of the single crystal ingot 19.

On the basis of the foregoing summary of the process in Kito et al, there are clear differences from the present invention.

(1) Formation of the SiC film

In the present invention, as expressly set forth in claim 1, the SiC single crystal film is formed by a surface chemical reaction in which the substrate surface is subjected to carbonization or silicification.

By contrast, according to Kito et al, the SiC single crystal layer is deposited by CVD.

(2) Use of Partial Pressure

In the present invention, as expressly set forth in claim 1, the partial pressure of the raw material gas on the substrate surface is a given partial pressure higher by at least a predetermined rate than that of an impurity, thereby suppressing the impurity from reaching the substrate surface.

In Kito et al, there is no recognition that the use of partial pressures can prevent an impurity from reaching the substrate.

(3) Effect of the SiC film

In the present invention, as expressly stated in the claim, the SiC single crystal film and its parameters for formation, namely the use of partial pressure to prevent an impurity from reaching the substrate surface, is used to prevent the substrate from being etched by an impurity gas.

On the other hand, the SiC base layer in Kito et al is used to permit high temperature growth of an (0001) $\alpha$-type SiC single crystal ingot. Specifically, the $\alpha$ phase of SiC is a high-temperature stable phase. Therefore, in order to form the (0001) $\alpha$-type SiC single crystal, the substrate temperature must be 1500°C or higher, as disclosed in. Kito et al. Thus, upon the deposition of (0001) $\alpha$-type SiC single crystal by the sublimation-recrystallization method, the single crystal double layers of the (0001) $\alpha$-type and (111) cubic SiC deposited by CVD is used to provide the necessary heat resistance for growth of the ingot. There is no concern with preventing etching of the surface or with preventing impurities from reaching the substrate surface.

The Examiner admits only to the failure of Kito et al to supply a raw material in the vicinity of the surface of the substrate at partial pressures that suppress an impurity from reaching the surface. The Examiner looks to Cook et al for a teaching of this admitted deficiency.

**Cook et al**

Cook et al concerns a process for achieving high deposition rates in semiconductor processes. As to impurities, Cook et al merely discloses that the amount of impurities in the film deposited by CVD may be controlled. There is no disclosure with respect to the problem of etching of the substrate (which is to be covered by the film) by the impurities contained in the raw material gas. Further, there is no teaching of a solution to that problem. Moreover, the details of the claims that are missing from Kito et al, are nowhere taught in Cook et al.

For example, Cook et al discloses at col. 7, line 66-col. 8, line 36 that the impurity concentration in the film that is deposited by CVD can be controlled. Cook et al states at col. 8, line 17 that the amount of impurities is proportional to the partial pressure of the impurity gas, the rate of reaction or entrapment of the impurities during deposition. Specifically, as a method of reducing the impurities in the film deposited by CVD, the following steps are disclosed in Cook et al.

(a) The concentration of the raw material gas among the gases above the substrate surface is increased to thereby reduce the partial pressure of the impurity gas above the substrate surface;

(b) The impurity gas is removed by increasing the gas flow rate; and

(c) The deposition rate is increased.

As described above, Cook et al merely discloses the reduction of the concentration of impurities present in the film deposited by CVD. Cook et al does not disclose that the substrate is etched by the impurities contained in the raw material gas when the film is deposited by CVD. More importantly, there is no description of the technique for preventing the substrate surface from being etched prior to film deposition by CVD. Accordingly, Cook et al is clearly different from the present invention and does not remedy the deficiencies of Kito et al.

The Examiner admits that Cook et al and Kito et al are silent with respect to the raw material in the vicinity of the surface of the substrate, as claimed, and attempts to remedy this deficiency by referring to routine experimentation. However, to even conduct such experimentation, the problem must be identified. As already noted, there is no recognition of the problem solved by the Applicants.

Finally, the focus of Cook et al and of Kito et al are so different that one of ordinary skill would not be motivated to combine them in a manner that would lead to the present invention.

Kito et al is concerned with growing a SiC ingot, while Cook et al is concerned with depositing films. Nothing in either reference would lead one skilled in the art to adapt Kito et al to incorporate the film process of Cook et al. Even if the Examiner persists in asserting such motivation, for the reasons given, the combination still does not lead to the present invention.

**Claims 2 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kito et al (6,110,279) in view of Cook et al (6,352,594) and further in view of Funato et al (5,882,807).** This rejection is traversed for at least the following reasons.

**Funato et al**

Funato et al discloses a method of depositing the SiC film by CVD on the surface of the Si-impregnated SiC substrate. Funato et al does not remedy the deficiencies already noted in the combination of Kito et al and Cook et al, as will be clear from the following analysis. Moreover, the disclosed method in Funato et al is not adequate to teach even the steps of the dependent claims taken in isolation.

Funato et al discloses a substrate heating activity that comprises two successive steps, the condition in each step is as follows:

First step: degassing the substrate at a pressure of 1 Torr or less and heating at a temperature of 600-850°C at a heating rate of 5-50°C/min.

Second step: introducing a non-oxidative gas until the pressure reaches 50-760 Torr and heating to 1000-1290°C at a heating rate of 5-50°C/min.

The first step is carried out to remove oxygen adsorbed to the Si-impregnated SiC substrate. In this sense, the substrate temperature must be heated to 600°C or higher. When the substrate temperature is not lower than 850°C, Si in the Si-impregnated SiC substrate is evaporated under the reduced pressure and pores tend to be easily produced in the SiC substrate. These pores result in cause of the reduction in adhesion of the SiC film, which is deposited by CVD, to the SiC substrate. In the example, the substrate temperature is selected to be 800°C and the substrate is maintained at that temperature for 30 minutes.

The second step involves elevating the temperature to a level required for the SiC film to be is deposited by CVD on the surface of the Si-impregnated SiC substrate. In the disclosed example, prior to supply of the raw material gas for deposition of SiC, the substrate is held for 30 minutes at a reached temperature (1000-1265°C).

The temperature elevation rate is 5-50°C/mm in both of the first and the second steps. If the temperature elevation rate exceeds 50°C/mm, thermal stress may be produced in the SiC substrate, which tends to cause cracks in the substrate. If the temperature elevation rate is lower than 5°C/mm, it will take a long time before a desired temperature is achieved. This impairs yield and productivity. From the above, the temperature elevation rate preferably falls within a range between 10-30°C/min.

In the Office Action (paragraph 9), the Examiner points out that the temperature reached in the first step of Funato et al reads on the "etching start temperature (Te) of the substrate surface" in the claimed invention and that the temperature reached in the second step reads on the temperature at which SiC is formed by substrate surface reaction (not formed by deposition such as CVD). Furthermore, the Examiner points out that the reached temperature of 600-850°C in the first step disclosed in Funato et al is similar to 800°C described in the present specification (page 15, lines 6-7).

However, as will be explained below, Funato et al and the present invention are greatly different in structure. Furthermore, upon selection of the above-mentioned temperature, background physical and chemical phenomena are totally different from each other. As a result, it is would not be possible for one skilled in the art to derive the present invention from the disclosure of Funato et al, taken alone or in combination with Kito et al and/or Cook et al.

The most explicit and important difference between the constituent elements of Funato et al and the present application is as follows. According to Funato et al, the object on which the SiC film is to be is deposited is a Si-impregnated SiC substrate. According to the present invention, the object is a substrate, such as a Si substrate, having a chemical nature of being etched by impurity gas components contained in the atmosphere upon deposition of the SiC film. This difference in the object causes the different physical and chemical phenomena on the deposition of SiC film by CVD. Consequently, the selection of the temperature and other conditions must be quite different in several respects.

First, there is a clear difference between the temperature in the first step of the Funato et al and the "etching start temperature (Te) of the substrate surface" in the present invention.

As described above, the temperature reached in the first step of Funato et al is a temperature sufficient to remove oxygen adsorbed to the Si-impregnated SiC substrate prior to

formation of the SiC film by CVD. Therefore, in order to sufficiently remove oxygen, it is essential that the substrate be maintained at that temperature for a necessary and sufficient time duration. On the other hand, the "etching start temperature (Te) of the substrate surface" in the present invention is a temperature at which the substrate starts to be etched by the impurity gas. The physical and chemical phenomena occurring at the temperature is quite different from the phenomena in the first step of Funato et al.

In addition, in order to fully exhibit the effect (effect of improving the adhesion of the SiC film to the substrate by removal of the adsorbed oxygen) described in Funato et al, it is indispensable to maintain the substrate at the temperature reached in the first step for a predetermined time. On the other hand, in the present invention, it would be inconceivable to maintain the substrate for a predetermined time at the "etching start temperature (Te) of the substrate surface."

Furthermore, the reason for selection of the temperature elevation rate is different as follows:

Selection of the temperature elevation rate in Funato et al is made considering the thermal stress induced in the Si-impregnated SiC substrate and the productivity. On the other hand, selection in the present invention aims to minimize the etching of the substrate. In this respect, the preferred temperature elevation rate is different. Specifically, Funato describes that the temperature elevation rate preferably falls within a range of 10-30°C/mm. On the other hand, in the present invention, as illustrated in Fig. 3 or 4, a high temperature elevation rate is preferable although the tendency of saturation is observed.

As described above, Funato et al is quite different from the technical concept of the present invention. Thus, considered alone or even combined with Kito et al and/or Cook et al, one skilled in the art would not be led to the present invention from Funato et al.

***Conclusion***

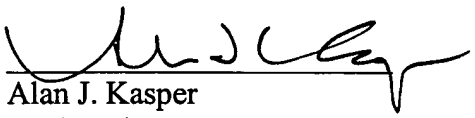
The Examiner has asserted that the present invention can readily be taught by a combination of the disclosures of the cited references. However, as described previously, there are significant differences between the prior art and the claimed invention, thus making the Examiner's position wholly unsupportable. That is, Kito et al and Cook et al disclose no more than the deposition of SiC film by CVD. Each of the cited references neither discloses nor

suggests the basic purpose or elements of the present invention, i.e., the technique of forming the SiC film by surface chemical reaction of the substrate in order to prevent etching by impurities. As described above, Funato et al is quite different in technical concept from the present invention and does not remedy the deficiencies of Kito et al or Cook et al.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Alan J. Kasper
Registration No. 25,426

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE

23373
PATENT TRADEMARK OFFICE

Date: July 11, 2003

## APPENDIX

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

**IN THE SPECIFICATION:**

**The specification is changed as follows:**

**Page 9, full paragraph No. 5,**

As the substrate, use can be made of Si, SiC, titanium carbide, [sapphire], diamond, or the like. The temperature at which the single crystal SiC layer is formed falls within the range between about 1000 and 1100°C in case where a Si substrate is used as the substrate. By heating the substrate to the above-mentioned temperature under existence of the substance containing C or C and Si, the single crystal SiC layer with high-quality having a film thickness of about 10 nm can relatively easily be formed (for example, see C. J. Mogab et al. Journal of Applied Physics Vol. 45 (1974) P1075-).

**Page 10, full paragraph No. 4,**

In the above-mentioned state, if the surface of the substrate 101 is etched by the impurity, molecules or atoms 103 constituting the substrate are detached or released from the substrate surface. Those molecules or atoms thus detached are monitored by using a quadrupole mass spectrometer 104. Herein, the etching start temperature Te is a temperature at which molecules or atoms derived from the composition of the substrate start to be detected. For example, if a Si substrate is employed, the etching start temperature Te corresponds to a temperature at which molecules or atoms derived from Si start to be detected. [Alternatively, if a sapphire substrate is used, the etching start temperature Te corresponds to a temperature at which molecules or atoms derived from Al start to be detected.]

**IN THE CLAIMS:**

**Claims 6-9 are canceled without prejudice or disclaimer.**

**The claims are amended as follows:**

Claim 1. (Amended). A method for manufacturing a single crystal SiC on a substrate having a surface, the substrate including at least one of Si or C, the method comprising the steps of:

a first step of [forming] coating the substrate with a thin single crystal SiC layer [on the surface] by heating the substrate under existence of a raw material containing C or Si, or C and Si to induce surface chemical reaction between said raw material and Si or C contained in the substrate, thereby forming the thin single crystal film; and

a second step of depositing SiC on the single crystal SiC layer, which is formed in the first step, by the vapor phase growth method or the liquid phase growth method;

the first step [of forming the single crystal SiC layer] being carried out in the manner such that the raw material is supplied in the vicinity of the surface of the substrate, and that the raw material in the vicinity of the surface of the substrate is given a partial pressure higher at least by a predetermined rate than that of an impurity, thereby suppressing the impurity from reaching the surface of the substrate and preventing the surface of the substrate from being etched by the impurity.

Claim 2. (Amended). A method as claimed in claim 1, wherein:

heating in the first step [of forming the single crystal SiC layer] comprises a temperature elevating step of elevating the temperature of the substrate from a first temperature Te at which etching of the surface of the substrate by the impurity is started to a second temperature not lower than a temperature at which the single crystal SiC layer is formed, the temperature elevating step being carried out on such a condition that the partial pressure of the raw material is adjusted to a level not lower than 100 times that of the impurity, and

the temperature elevating step being carried out by selecting at least one of a temperature elevating rate and a temperature elevating time within a range such that the density and the size of a defect such as etch pits or dome-like protrusions is suppressed to prevent occurrence of a planar defect on SiC which is deposited on the single crystal SiC layer by the vapor phase growth method or the liquid phase growth method.

Claim 3. (Amended) A method as claimed in claim 1, wherein:

at least one material selected from the group consisting of $C_nH_{2n}$ ($2 \leq n \leq 3$), $C_nH_{2n+2}$ ($1 \leq n \leq 3$), $C_nH_{2n-2}$ ($1 \leq n \leq 3$), $CCl_4$, $CHF_3$, and $CF_4$ is used as the material containing C and used in the in the first step for forming the single crystal SiC layer.

Claim 4. (Amended) A method as claimed in claim 1, wherein:

at least one material selected from the group consisting of $SiH_2Cl_2$, $SiH_4$, $SiCl_4$, $SiHCl_3$, $Si_2H_6$, and $Si_2Cl_6$ is used as the material containing Si and used in the first step of forming the single crystal SiC layer in addition to the material containing C.

**Claim 10 is added as new claims.**